MODIFIED ENERGY AND AREA EFFICIENT CARRY SELECT ADDER USING BEC ON A RECONFIGURABLE HARDWARE

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***Abstract*—**Carry Select Adder (CSLA) is one of the widely used digital components in digital integrated circuit design. The proposed design is implemented using BEC and RCA structure with Cin=0. Based on this modification 8-, 16-, 32-, and 64-b square-root CSLA (SQRT CSLA) architecture have been developed and compared with the regular SQRT CSLA architecture. The proposed design has reduced area and energy as compared with the regular SQRT CSLA with only a slight increase in the delay. The compared results show that the modified SQRT CSLA has a slightly larger delay (31.42%), but the area and energy of the 64-b modified SQRT CSLA are significantly reduced by 10.16% and 2.10% respectively.

Index Terms—Application-specific integrated circuit (ASIC), area-efficient, CSLA, low power
Multiplexer, performance, adder, VLSI and data paths.

I-INTRODUCTION

In rapidly growing mobile industry, faster units are not the only concern but also smaller area and less energy become major concerns for design of digital circuits. The design of high-speed and low-power VLSI architectures needs efficient arithmetic processing units, which are optimized for the performance parameters, namely, speed and energy consumption. Adders are the key components in general purpose microprocessors and digital signal processors. The CSLA is used in many computational systems to alleviate the problem of carry propagation delay by independently generating multiple carries and then select a carry to generate the sum. However, the CSLA is not area efficient because it uses multiple pairs of Ripple Carry Adders (RCA) to generate partial sum and carry by considering carry input cin=0 and cin=1, then the final sum and carry are selected by the multiplexers (mux). In digital adders, the speed of addition is limited by the time required to propagate a carry through the adder. The basic idea of this work is to use

Binary to Excess-1 Converter (BEC) instead of RCA with cin=1 in the regular CSLA to achieve lower area and energy consumption. The main advantage of this BEC logic comes from the lesser number of logic gates than the N-bit Full Adder (FA) structure. Ramkumar and Harish 2012 propose BEC technique which is a simple and efficient gate level modification to significantly reduce the area and power of square root CSLA.

In mobile electronics, reducing area and energy consumption are key factors in increasing portability and battery life. In this paper we proposed Modified Carry Select-Adder (MCSA) architecture to reduce area and energy with minimum speed penalty .The MCSA is designed by using single RCA and Binary to Excess-1 Converter (BEC) instead of using dual RCAs.

II-BASIC ADDER BLOCKS

The AND, OR, and Inverter (AOI) implementation of an XOR gate is shown in Figure 1. The gates between the dotted lines are performing the operations in parallel and the numeric representation of each gate indicates the delay contributed by that gate. All gates to be made up of AND, OR, and Inverter in delay and area evaluation methodology, each having delay equal to 1 unit and area equal to 1 unit. We then add up the number of gates in the longest path of a logic block that contributes to the maximum delay. The area evaluation is done by counting the total number of AOI gates

required for each logic block. Based on this approach, the CSLA adder blocks of 2:1 mux, Half Adder (HA), and FA are evaluated and listed in Table I.

Fig 1 Half Adder

TABLE I
DELAY AND AREA COUNT OF THE BASIC BLOCKS OF CSLA

Adder blocks	Delay	Area
XOR	3	5
2:1 Mux	3	4
Half adder	3	6
Full adder	6	13

III-RIPPLE CARRY ADDER

A ripple carry adder is a logic circuit shown in figure 2. In which multiple full adder circuits can be cascaded in parallel to add an N-bit number. For an N- bit parallel adder, there must be N number of full adder circuits. They carry-out of each full adder in succeeding next most signi ficant full adder. In a ripple carry adder the sum and carry out bits of any half adder stage is not valid until the carry in of that stage occurs. Propagation delays inside the logic circuitry is the reason behind this. Propagation delay is time elapsed between the application of an input and occurance of the Corresponding output. Similarly the carry propagation delay is the time elapsed between the application of the carry in signal and the occurrence of the carry out (Cout) signal. Sum out S0 and carry out Cout of the Full Adder 1 is valid only after the propagation delay of Full Adder 1. In the same way, Sum out S3 of the Full Adder 4 is valid only after the joint propagation delays of Full Adder 1 to Full Adder 4. In simple words, the final result of the ripple carry adder is valid only after the joint propagation delays of all full adder circuits inside it.

Si = Ai xor Bi xorCi

Ci+1 = Ai Bi + (Ai + Bi) Ci; where i = 0, 1, …,n-1

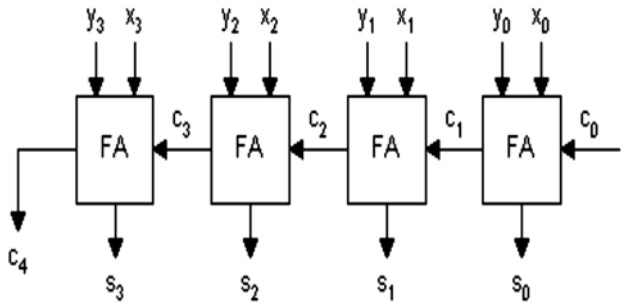

Fig 2 Ripple Carry Adder

III-BINARY TO EXCESS CONVERTER (BEC)

BEC is a circuit used to add 1 to the input numbers. In BEC, numbers are represented as decimal digits, and each digit is represented by four bits as the digit value plus and numeral system. A circuit of 4-bit BEC and the truth table is shown in Figure 3 and Table 2 respectively. An N+1 bit BEC replaces the N bit RCA. BEC is instead of the RCA with reduce the area and energy consumption of the regular CSLA. One input of the 8:4 mux gets as it input (B3, B2, B1, and B0) and another input of the mux is the BEC output. This produces the two possible partial results in parallel and the mux is used to select either the BEC output or the direct inputs according to the control signal Cin. In earlier BEC was used on some older computers as well as in cash registers and hand held portable electronic calculators of the 1970's, among other uses.

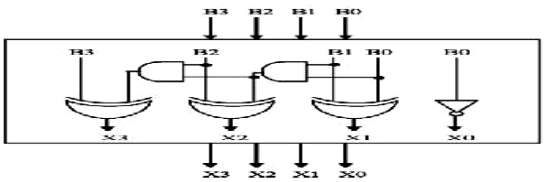

Fig 3 BEC

X0 = ~B0

X1 = B0 ^ B1

X2 = B2 ^ (B0 & B1)

X3 = B3 ^ (B0 & B1 & B2)

Table 2. Truth table of 4-bit Binary to Excess-1 logic

Binary	Excess-1

0000	0001
0001	0010
0010	0011
0011	0100
0100	0101
0101	0110
0110	0111
0111	1000
1000	1001
1001	1010
1010	1011
1011	1100
1100	1101
1101	1110
1110	1111
1111	0000

VI-ASIC IMPLEMENTATION RESULTS

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The various adders are designed using Verilog language in Xilinx ISE Navigator 14.1 and all the simulations are performed using Xilinx ISim simulator. The performance of proposed MCSA is analysed and compared against the SQRT CSLA designs. The number of gates used in the design indicates the area of design. The energy consumption

REGULAR 16-B SQRT CSLA

In 16-bit CSLA carry in is applied to 1:0 RCA and carry out is propagated to select line of mux and RCA is selected by depend upon the carry out value so if carry out is 0 then first RCA is selected and otherwise RCA is select then process is continued and increase the bit number in, RCA in every stage. 16 bit sum is obtained in this structure but area is larger because number of gate is large due to number of full adder. The structure of the 16-bit regular SQRT CSLA is shown in Figure 4. The one set of 2-bit RCA in group 2 has 2 FA for Cin=1 and the other set has 1 FA and 1 HA for Cin=0.

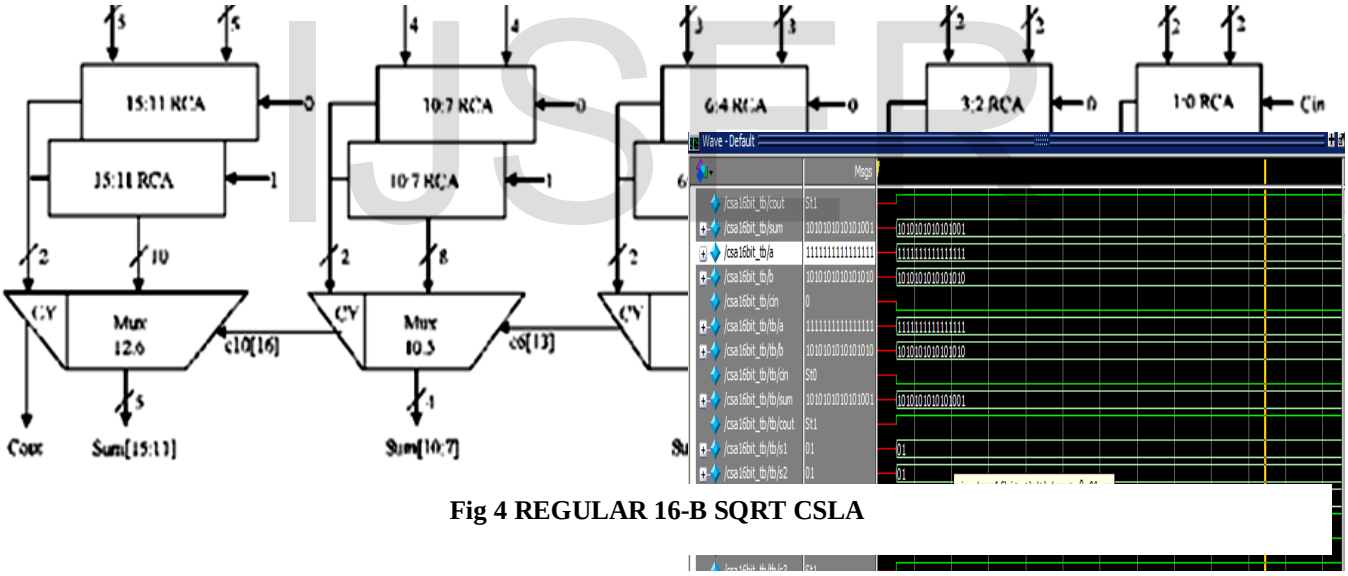

Fig 4 REGULAR 16-B SQRT CSLA

MODIFIED 16-B SQRT CSLA

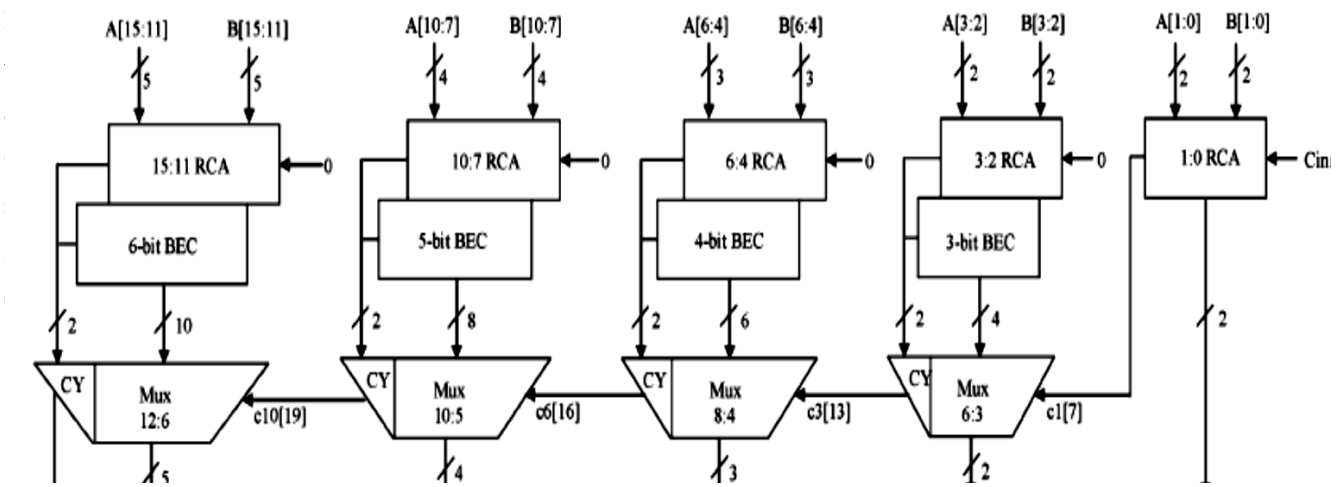

Fig 5 MODIFIED 16-B SQRT CSLA

is measured in terms of total energy and dynamic energy. The speed of the adder is estimated by the delay involved in the design. It can be seen from Table 3 that area and energy consumption of MCSA is less than that of SQRT CSLA, whereas delay is more in MCSA. This shows that area and energy consumption of MCSA is reducing at the cost of small decrease in speed. As the number of gates used in the design of MCSA are fewer than the SQRT CSLA. The reduced number of gates of the MCSA offers a great advantage in the reduction of area and total energy consumption.

Fig 6 Simulation result of Regular 16-B SQRT CSLA

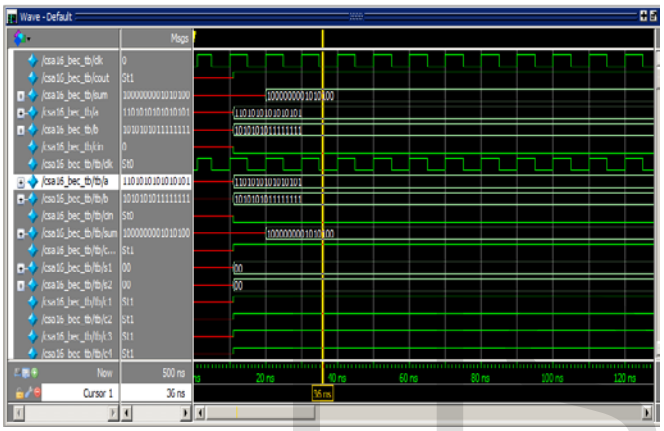

Fig 7 Simulation result of Modified 16-B SQRT CSLA

Table 3

Bit	Adder	Delay(ns)	Area (LUT)	Dynamic Energy (e)	Total Energy (e)	Energy-Delay Product
8	CSA	3.113	21	0.009	1.302	4.053
	BEC	8.277	19	0.007	1.300	10.76
16	CSA	4.225	61	0.017	1.310	5.534
	BEC	9.587	41	0.015	1.308	12.53
32	CSA	5.242	124	0.035	1.328	6.961
	BEC	11.94	82	0.031	1.325	15.82
64	CSA	6.286	202	0.071	1.365	8.580
	BEC	16.37	179	0.065	1.359	22.24

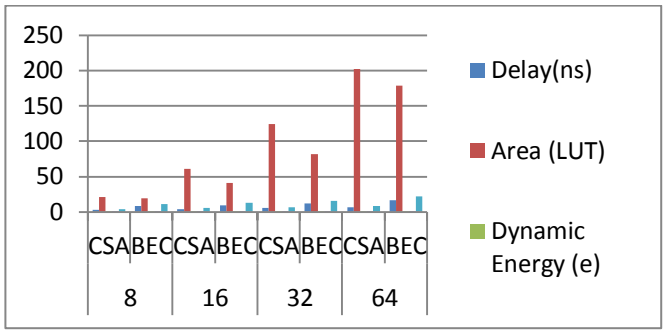

Fig 8 Comparison between different logic style in terms of delay,Area,Power.

VII-CONCLUSION

In this paper a simple approach is proposed to reduce the area and energy of SQRT CSLA architecture. The reduced number of gates of this work offers the great advantage in the reduction of area and also the total energy. The compared results show that the modified SQRT CSLA has a slightly larger delay (31.42%), but the area and energy of the 64-b modified SQRT CSLA are significantly reduced by 10.16% and 2.10% respectively.The energy-delay product of the proposed design show a decrease for 16-, 32-, and 64-b sizes which indicates the success of the method and not a mere tradeoff of delay for energy and area. The modified CSLA architecture is therefore, low area, low energy, simple and efficient for VLSI hardware implementation. But the disadvantage of BEC method is that the delay is increasing than the regular CSLA.We can use any digital circuits instead of RCA to reduced the delay,area, energy in SQRT CSLA.

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